



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

Am

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,161	08/08/2001	Stephen Clark Purcell	69102 278147	3092

20350 7590 06/14/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER

FERRIS III, FRED O

ART UNIT PAPER NUMBER

2128

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/925,161

Applicant(s)

PURCELL ET AL.

Examiner

Fred Ferris

Art Unit

2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. *Claims 1-37 have been presented for examination based on applicant's disclosure filed 8 August 2001. Claims 1-37 have been rejected by the examiner.*

Drawings

2. *Applicant's drawings submitted on 2 October 2001 have been approved by the examiner.*

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. ***Claims 1-26 are rejected under 35 U.S.C. 101 because the claimed invention is drawn to non-statutory subject matter.***

Per independent claims 1 and 14: The Examiner submits that method claims 1 and 14, as written, are merely drawn to a mental process for accumulating initial input values, since the language of the claims can be interpreted as meaning the method is carried out by a mental process augmented (calculated) using pencil and paper. (i.e. not a machine or computer process)

MPEP 2111 [R-1] recites the following:

***"2111 [R-1] Claim Interpretation; Broadest Reasonable Interpretation
CLAIMS MUST BE GIVEN THEIR BROADEST REASONABLE
INTERPRETATION***

During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000).< Applicant always has the

Art Unit: 2128

opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In *re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969) (Claim 9 was directed to a process of analyzing data generated by mass spectrographic analysis of a gas. The process comprised selecting the data to be analyzed by subjecting the data to a mathematical manipulation. The examiner made rejections under 35 U.S.C. 101 and 102. In the 35 U.S.C. 102 rejection, the examiner explained that the claim was anticipated by a mental process augmented by pencil and paper markings. The court agreed that the claim was not limited to using a machine to carry out the process since the claim did not explicitly set forth the machine. The court explained that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim, to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The court found that applicant was advocating the latter, i.e., the impermissible importation of subject matter from the specification into the claim.). See also *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997) (The court held that the PTO is not required, in the course of prosecution, to interpret claims in applications in the same manner as a court would interpret claims in an infringement suit. Rather, the "PTO applies to verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in applicant's specification.")"

The Examiner further submits that, in view of the language of the claims, Applicant's have merely claimed a manipulation of abstract ideas by a mental process and have not specifically set forth a machine or computer process.

Section 2106 [R-2] (Patentable Subject Matter — Computer-Related Inventions) of the MPEP recites the following:

"In practical terms, claims define nonstatutory processes if they:
– consist solely of mathematical operations without some claimed practical application (i.e., executing a "mathematical algorithm"); or
– simply manipulate abstract ideas, e.g., a bid (*Schrader*, 22 F.3d at 293-94, 30 USPQ2d at 1458-59) or a bubble hierarchy (*Warmerdam*, 33 F.3d at 1360, 31 USPQ2d at 1759), without some claimed practical application."

In this case, claims 1 and 14 are simply drawn to the manipulation of abstract ideas by the mental process of accumulating input values from an arbitrary N-length string. Dependent claims 2-13 and 15-26 inherit the defects of the claims from which they depend.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,571,268 issued to Giacalone et al in view of U.S. Patent Application Publication 2002/0039386 A1 issued to Han et al.

Independent claim 1, for example, is drawn to:

method of constructing an accumulator, comprising:
simulating layered tree structure containing intermediate accumulation data;
programming structure to direct data to inputs from arbitrary length string so
accumulator maintains order of operations for simulated layers.

Regarding independent claim 1: Giacalone teaches constructing an accumulator inclusive of a layered tree structure (CL5-L55-67, CL6-L43-67, Figs. 1, 2) controlling flow of the accumulation data and a programmed (i.e. directed) structure (CL5-L39-67,

CL15-L17-55, CL23-L3-53, Figs. 1, 7A, 17A-C) for controlling the string length inputs (CL7-L61 to CL8-L5, Fig. 2) and maintaining control of the layers within the tree structure. (CL11-L29 to CL12-L7, Figs. 4A-C).

Giacalone does not explicitly disclose a layered tree structure configured to contain the intermediate accumulation result.

Han also teaches constructing an accumulator inclusive of a layered tree structure, but further teaches a tree structure that is configured to buffer (contain) the intermediate accumulation results (Para: 0060, 0053, Fig. 11).

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Giacalone relating to constructing an accumulator inclusive of a layered tree structure controlling and buffering the accumulation data, with the teachings of Han relating to a tree structure that is configured to buffer (contain) the intermediate accumulation results, to realize the elements of the claimed invention. An obvious motivation exists since, in this case, the Giacalone reference teaches to the Han reference, and the Han reference teaches to the Giacalone reference. Specifically, both Giacalone and Han teach an accumulator design including a controlling tree structure and both are used in the same technological arena as noted above. Giacalone teaches to Han because Giacalone teaches a layered tree structure for controlling and buffering the accumulation data as does Han (See: Giacalone, Summary of Invention). Han teaches to Giacalone because Han specifically teaches a tree structure that is configured to buffer (contain) the intermediate accumulation results. (See: Han: 0060, Fig. 11) Further, the level of skill required by an

artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Giacalone/Han, Background/Abstract) Accordingly, a skilled artisan tasked with realizing an accumulator inclusive of a layered tree structure configured to buffer the intermediate accumulation results, and having access to the teachings of Giacalone and Han, would have knowingly modified the teachings of Giacalone with the teachings of Han (or visa versa) to realize the claimed elements of the present invention while reducing the cost and development time.

Regarding dependent claims 2-4: *Giacalone teaches using a first and second (i.e. equivalent to left and right) accumulator memory bank (CL28-L59-67, Figs. 20-24) processed in first in, first out (i.e. FIFO) order (CL3-L35-41).*

Regarding dependent claims 5-13: *Giacalone teaches controlling a first and second (i.e. a first and second source, equivalent to left and right) accumulator memory bank (CL28-L59-67, Figs. 20-24) and directing (redirecting and selecting) the result into various fields. (CL23-L31-47, Fig. 17C) Selecting "zero" would obviously be necessary in order to flush (clear) the memory bank. Han discloses single adder control (Fig. 6) and would have knowingly been incorporated by a skilled artisan using the reasoning cited above.*

Regarding independent claim 14: *As cited above, Giacalone renders obvious the limitations relating to constructing an accumulator inclusive of a layered tree structure (CL5-L55-67, CL6-L43-67, Figs. 1, 2) controlling flow of the accumulation data and a programmed (i.e. directed) structure (CL5-L39-67, CL15-L17-55, CL23-L3-53, Figs. 1,*

7A, 17A-C) for controlling the string length inputs (CL7-L61 to CL8-L5, Fig. 2) and maintaining control of the layers within the tree structure. (CL11-L29 to CL12-L7, Figs. 4A-C) In addition, Giacalone teaches an accumulator method capable of accommodating larger arbitrary input values (i.e. N-length strings) (CL8-L3-5, Fig. 2) as recited as an additional element in independent claim 14.

Giacalone does not explicitly disclose a layered tree structure configured to contain the intermediate accumulation result.

Han also teaches constructing an accumulator inclusive of a layered tree structure, but further teaches a tree structure that is configured to buffer (contain) the intermediate accumulation results (Para: 0060, 0053, Fig. 11).

It would have been obvious to one having ordinary skill in the art at the time the claimed invention was made to modify the teachings of Giacalone relating to constructing an accumulator inclusive of a layered tree structure controlling and buffering the accumulation data, with the teachings of Han relating to a tree structure that is configured to buffer (contain) the intermediate accumulation results, to realize the elements of the claimed invention. An obvious motivation exists since, in this case, the Giacalone reference teaches to the Han reference, and the Han reference teaches to the Giacalone reference. Specifically, both Giacalone and Han teach an accumulator design including a controlling tree structure and both are used in the same technological arena as noted above. Giacalone teaches to Han because Giacalone teaches a layered tree structure for controlling and buffering the accumulation data as does Han (See: Giacalone, Summary of Invention). Han teaches to Giacalone because Han specifically

teaches a tree structure that is configured to buffer (contain) the intermediate accumulation results. (See: Han: 0060, Fig. 11) Further, the level of skill required by an artisan to realize the claimed limitations of the present invention is clearly established by both references. (See: Giacalone/Han, Background/Abstract) Accordingly, a skilled artisan tasked with realizing an accumulator inclusive of a layered tree structure configured to buffer the intermediate accumulation results, and having access to the teachings of Giacalone and Han, would have knowingly modified the teachings of Giacalone with the teachings of Han (or visa versa) to realize the claimed elements of the present invention while reducing the cost and development time.

Regarding dependent claims 15-18: *Giacalone teaches using a first and second (i.e. equivalent to left and right) accumulator memory bank (CL28-L59-67, Figs. 20-24) processed in a first in, first out (i.e. FIFO) order (CL3-L35-41). Giacalone further teaches further teaches elements relating to controlling accumulator input delay (CL16-L8-55, Fig. 8, 7A), phase count (Figs. 2, 5, 8, i.e. odd/even input), and control fields (CL23-L53-67, CL25-L57-67, Figs 17C, 22)*

Regarding dependent claims 19-27: *Giacalone teaches controlling a first and second (i.e. a first and second source, equivalent to left and right) accumulator memory bank (CL28-L59-67, Figs. 20-24) and directing (redirecting and selecting) the result into various fields. (CL23-L31-47, Fig. 17C) Selecting "zero" would obviously be necessary in order to facilitate flushing (zeroing) the memory bank. Han discloses single adder control (Fig. 6) and would have knowingly been incorporated by a skilled artisan using the reasoning cited above. Giacalone further teaches bridge functions (CL13-L31-47)*

between stages (layers), accommodating sign extended input values (CL13-L48-63), and manipulating fields based on cycle functions (Table 7).

Regarding claims 28-37: This group of claims merely claims the apparatus for the same limitations as recited in accumulator method claims 1-27 and are therefore rejected using the same reasoning as previously recited above.

Conclusion

5. *The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.*

"Accelerating Pipelined Integer and Floating-Point Accumulations in Configurable Hardware with Delayed Addition Techniques", Luo et al, IEEE Transactions on Computers, Vol. 49, No. 3, March 2000 teaches floating point tree based accumulators.

"Architectures for Pipelined Wallace Tree Multiplier-Accumulators", Pang, IEEE CH2909-0/90/0000/0247, IEEE 1990 teaches floating point tree based accumulators.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the

Art Unit: 2128

examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

Fred Ferris, Patent Examiner
Simulation and Emulation, Art Unit 2128
U.S. Patent and Trademark Office
Randolph Building, Room 5D19
401 Dulany Street
Alexandria, VA 22313
Phone: (571-272-3778)
Fred.Ferris@uspto.gov
June 10, 2005

FL7
AW 2/28